Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 10-14 are pending in the application, with claim 10 being the independent claim. Claims 1-9 and 15-24 are sought to be withdrawn. Claim 11 is sought to be canceled without prejudice to or disclaimer of the subject matter therein. Claims 10 and 12 are sought to be amended. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Rejections under 35 U.S.C. § 102

Claims 10-14 were rejected under 35 U.S.C. § 102(a) as being anticipated by U.S. Patent No. 5,408,428 to Burgess et al. ("Burgess"). For the reasons set forth below, Applicants respectfully traverse this rejection.

Burgess is directed to a mask-programmable read only memory bit cell. (*See* abstract of Burgess). Burgess describes

> The ***single output pole*** of DPST switch 24 delivers the voltage level corresponding to the logic state of bit cell 16 (labeled V_{OUT})

(*See* Burgess at column 3, lines 28-30, emphasis added). Thus Burgess describes a "bit cell" that has a "single output". In contrast, independent claim 1, as amended, recites "a programmable memory cell ***for storing a plurality of values***, the memory cell

comprising.....***outputs*** coupled to the first and second supply potentials by said first and second metal interconnect structures, wherein each of said first and second metal interconnect structures can be programmed repeatedly by altering any one of the plurality of metal layers and any one of a plurality of via layers" (emphasis added). Applicants respectfully submit that Burgess fails to teach or suggest each and every element of independent claim 1. By virtue of the foregoing amendment, claim 11 has been cancelled thereby rendering its rejection moot. Dependent claims 12-14 are also not anticipated by Burgess for at least the same reasons as independent claim 10 from which they depend and further in view of their own respective features. Applicants therefore respectfully request that the Examiner reconsider and withdraw the rejection.

Claims 10-14 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,765,345 to Jai. P Bansal ("Bansal"). For the reasons set forth below, Applicants respectfully traverse this rejection.

Bansal is directed to a gate array core cell for VLSI ASIC devices. Bansal describes "the means to design gate array ASICS with comparable circuit density, performance, and power dissipation to the standard cell ASICs while reducing the mask cost and ASIC component fabrication time to about half of the standard cell ASICs." (*See* Bansal at column 2, lines 39-43).

Page 3 of the Office Action states:

> ...a programmable memory cell (fig. 3) for storing a value...

Applicants respectfully disagree. Bansal describes,

> FIG. 3 is a top view of a 2x2 block of the gate array core cells of the present invention, which illustrates the formation of rows and columns of the core region semiconductor ASIC chip

(*See* Bansal at column 3, lines 44-47). Applicants respectfully submit that nowhere does FIG. 3 of Bansal or its associated description teach or suggest "a programmable memory cell for storing a plurality of values" as recited in independent claim 1.

Page 3 of the Office Action also states:

> ...the memory cell comprising a first metal interconnect structure 5 (fig. 9) that traverses the plurality of vias; a second metal interconnect structure 6 (fig. 9) that traverses the plurality of metal layers using a second plurality of vias (fig. 9)...

Applicants respectfully disagree. In contrast to the above assertion by the Examiner, Bansal describes:

> The VDD bus 5 at metal M1 is connected to the source regions of the PMOS transistors using diffusion to metal contacts shown as shaded square shapes under the bus. Similarly source diffusion regions of the NMOS transistors are connected to the metal M1 GND bus 6.

(*See* Bansal at column 8, lines 31-36). Bansal does not describe VDD bus 5 or GND bus 6 of Fig. 9 as traversing a plurality of metal layers using a plurality of vias. Thus, nowhere does Bansal teach or suggest "a first metal interconnect structure that traverses the plurality of metal layers using a first plurality of vias; a second metal interconnect structure that traverses the plurality of metal layers using a second plurality of vias" as recited in independent claim 1. Bansal also fails to teach or suggest "outputs coupled to the first and second supply potentials by said first and second metal interconnect structures, wherein each of said first and second metal interconnect

structures can be programmed repeatedly by altering any one of the plurality of metal layers and any one of a plurality of via layers" as recited in independent claim 1, as amended. Applicants respectfully submit that Bansal fails to teach or suggest each and every element of independent claim 1. By virtue of the foregoing amendment, claim 11 has been cancelled thereby rendering its rejection moot. Dependent claims 12-14 are also not anticipated by Bansal for at least the same reasons as independent claim 10 from which they depend and further in view of their own respective features. Applicants therefore respectfully request that the Examiner reconsider and withdraw the rejection.

Double Patenting Rejection

On page 5 of the Office action, claims 10, 12-14 were rejected under the judicially created doctrine of obviousness-type double patent as being unpatentable over claims 1, 9, 14-16, 18-20, 30 of U.S. Patent No. 6,933,547. Applicants obviate these obviousness-type double patenting rejections based upon the terminal disclaimer submitted herewith. Accordingly, Applicants respectfully request that the rejection be withdrawn.

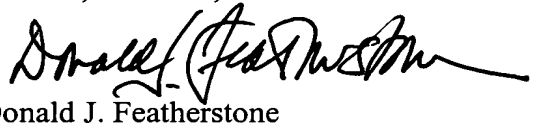
Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.



Donald J. Featherstone
Attorney for Applicants
Registration No. 33,876

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1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600
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